WHAT IS CLAIMED IS:

1. An interconnection structure of a semiconductor device having an interconnection locally provided with a stress concentration portion having tensile stress higher than that of another portion of said interconnection generated therein.

2. The interconnection structure of a semiconductor device according to claim 1, wherein said interconnection is provided with a dummy interconnection connected to an interconnection body, and said dummy interconnection is provided with said stress concentration portion.

3. The interconnection structure of a semiconductor device according to claim 2, wherein said dummy interconnection is formed of a via.

4. The interconnection structure of a semiconductor device according to claim 1, wherein the tensile stress is generated in said stress concentration portion by providing an insulating film having internal stress of compression, in proximity to said stress concentration portion or in contact with said stress concentration portion.

5. The interconnection structure of a semiconductor device according to claim 4, wherein said insulating film is a SiN film deposited by plasma CVD.

6. The interconnection structure of a semiconductor device according to claim 1, wherein the tensile stress in said stress concentration portion is not less than 200MPa nor more than 400MPa.